FIG. 1

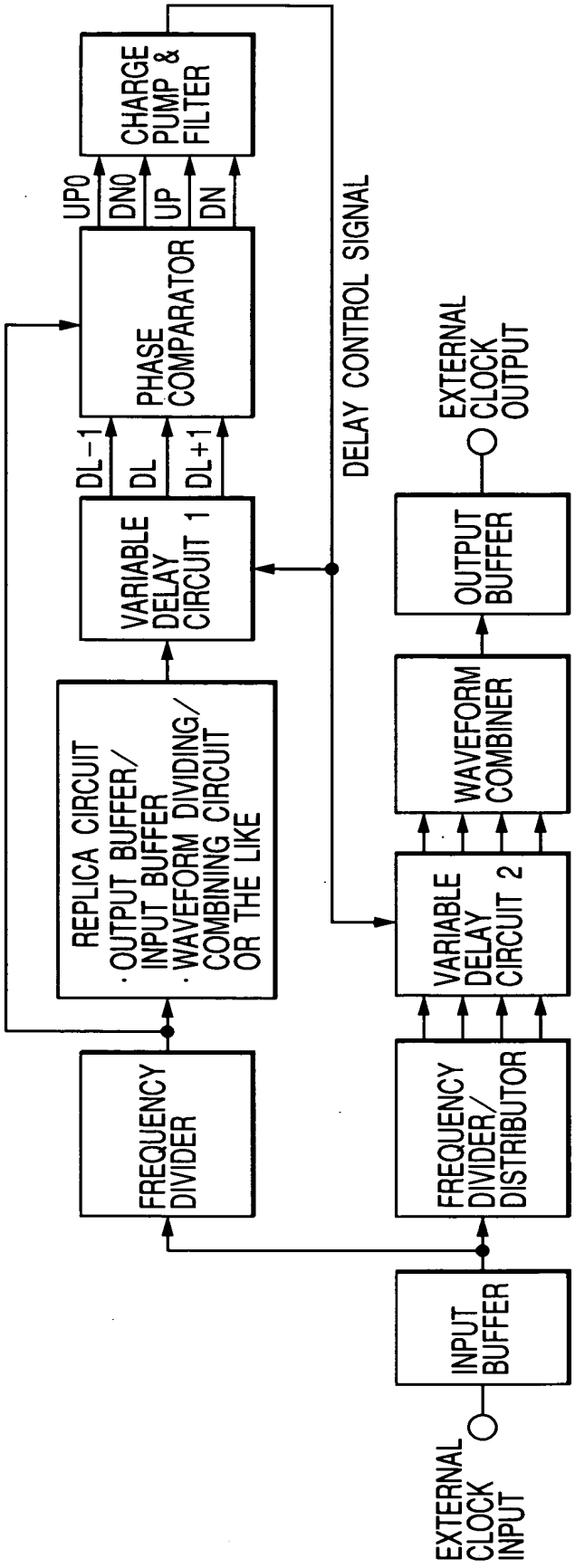

EXTERNAL CLOCK INPUT
INPUT BUFFER
FREQUENCY DIVIDER/ DISTRIBUTOR
FREQUENCY DIVIDER
VARIABLE DELAY CIRCUIT 2
VARIABLE DELAY CIRCUIT 1
REPLICA CIRCUIT ·OUTPUT BUFFER/ INPUT BUFFER ·WAVEFORM DIVIDING/ COMBINING CIRCUIT OR THE LIKE
WAVEFORM COMBINER
OUTPUT BUFFER
EXTERNAL CLOCK OUTPUT
DELAY CONTROL SIGNAL
DL-1
DL
DL+1
PHASE COMPARATOR
UP0
DN0
UP
DN
CHARGE PUMP & FILTER

FIG. 2

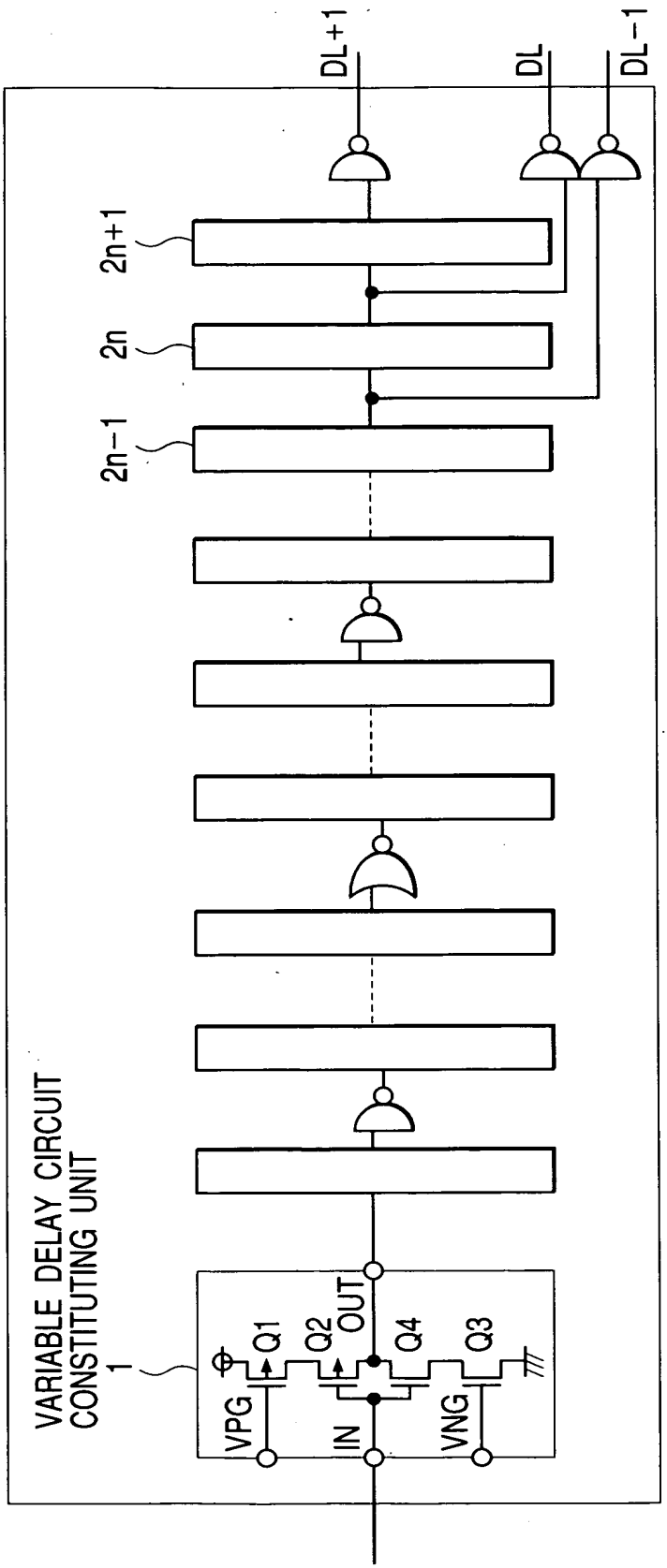

DL+1
DL
DL−1
2n+1
2n
2n−1
VARIABLE DELAY CIRCUIT CONSTITUTING UNIT
1
VPG
IN
VNG
Q1
Q2
OUT
Q4
Q3

FIG. 3

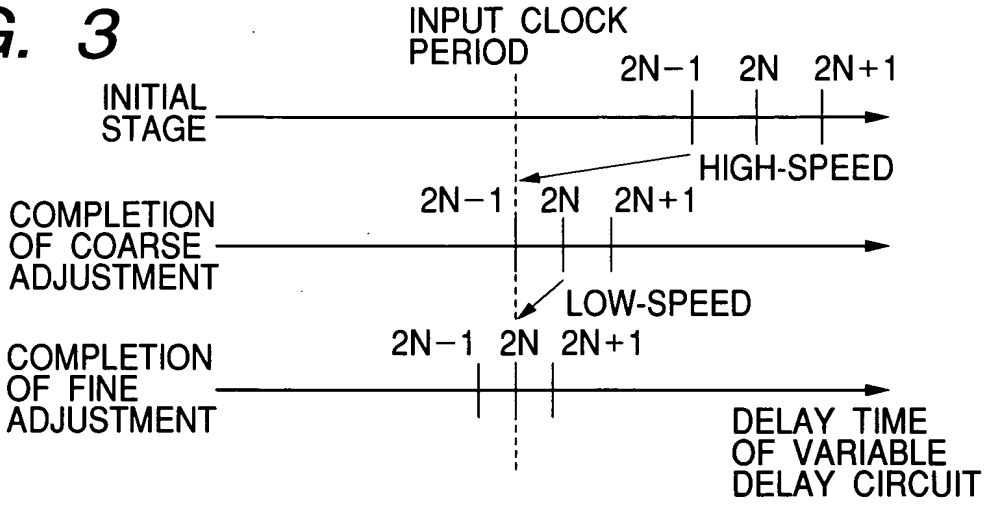


FIG. 4

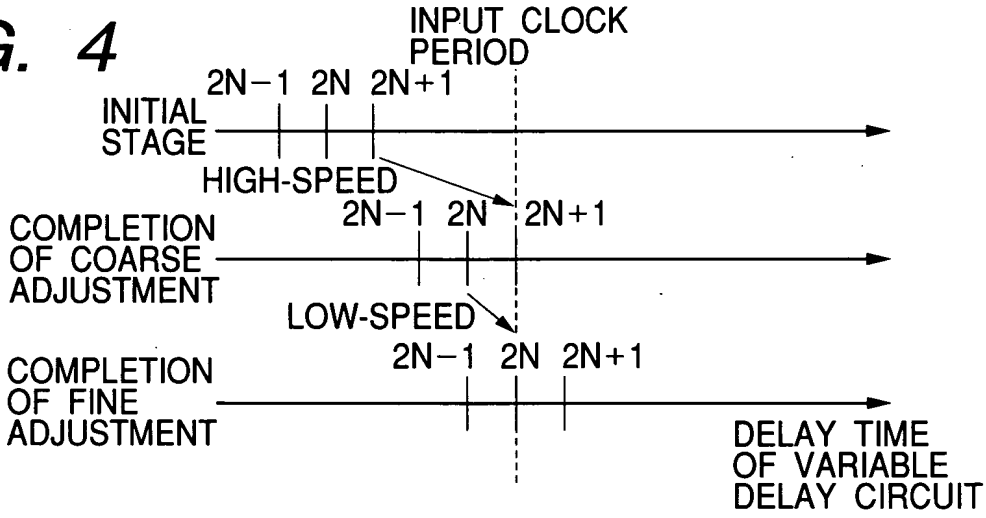


FIG. 5

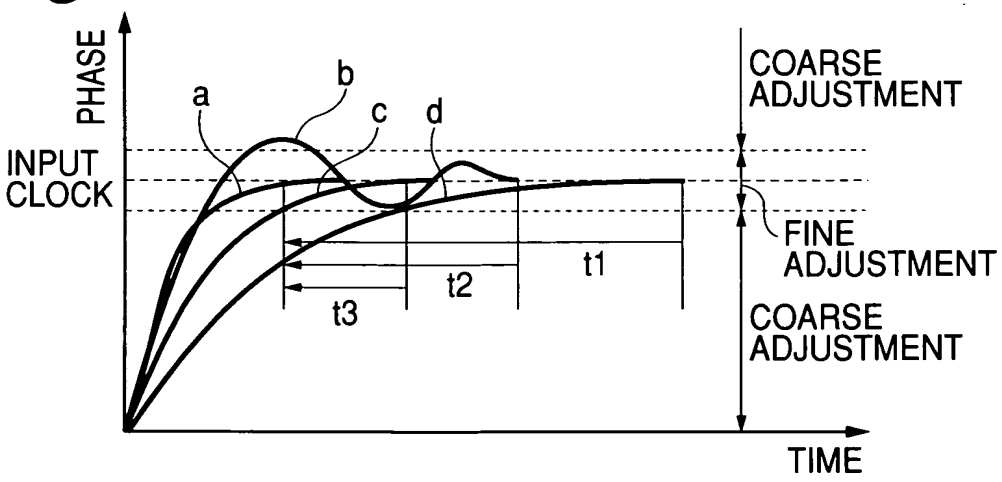


FIG. 6

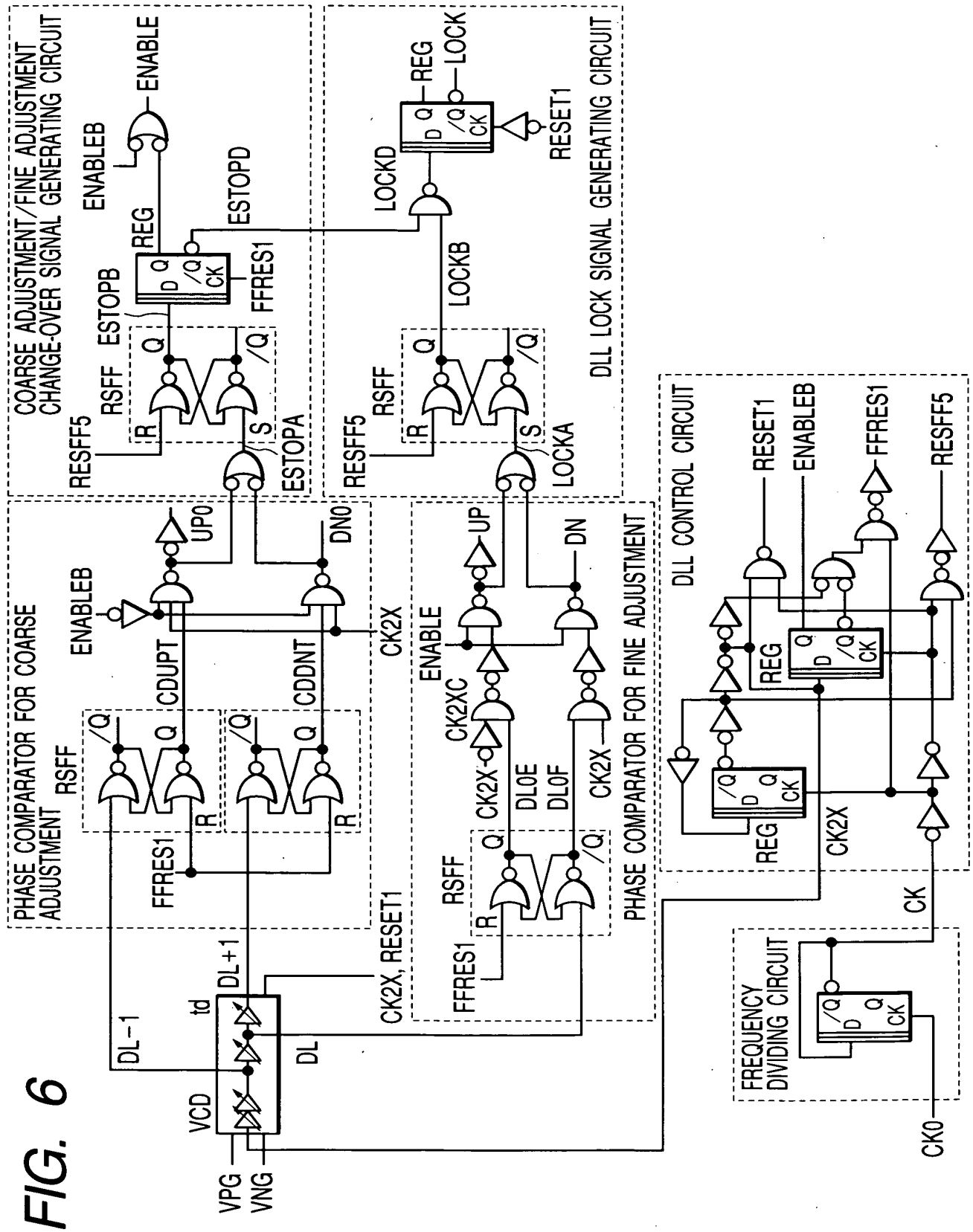

COARSE ADJUSTMENT/FINE ADJUSTMENT CHANGE-OVER SIGNAL GENERATING CIRCUIT
RESFF5
RSFF
ESTOPB
REG
ENABLEB
ENABLE
ESTOPD
FFRES1
ESTOPA
DLL LOCK SIGNAL GENERATING CIRCUIT
LOCKD
LOCKB
LOCKA
LOCK
RESET1
PHASE COMPARATOR FOR COARSE ADJUSTMENT
UP0
DN0
CDUPT
CDDNT
CK2X
FFRES1
CK2X, RESET1
PHASE COMPARATOR FOR FINE ADJUSTMENT
UP
DN
CK2XC
DL0E
DL0F
DL-1
DL
DL+1
td
VCD
VPG
VNG
DLL CONTROL CIRCUIT
FREQUENCY DIVIDING CIRCUIT
CK
CK0

FIG. 7

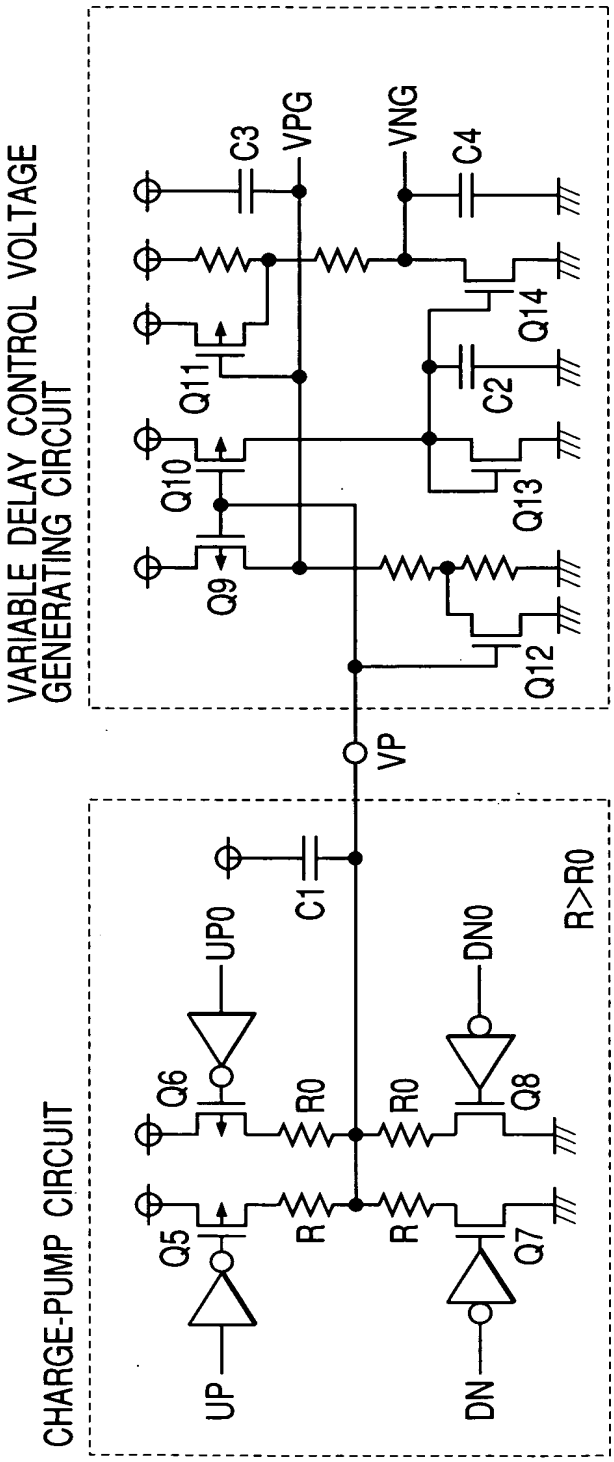

VARIABLE DELAY CONTROL VOLTAGE GENERATING CIRCUIT
C3
VPG
VNG
C4
Q14
Q11
C2
Q10
Q13
Q9
Q12
VP
CHARGE-PUMP CIRCUIT
C1
UP0
DN0
R>R0
Q6
R0
R0
Q8
Q5
R
R
Q7
UP
DN

FIG. 8

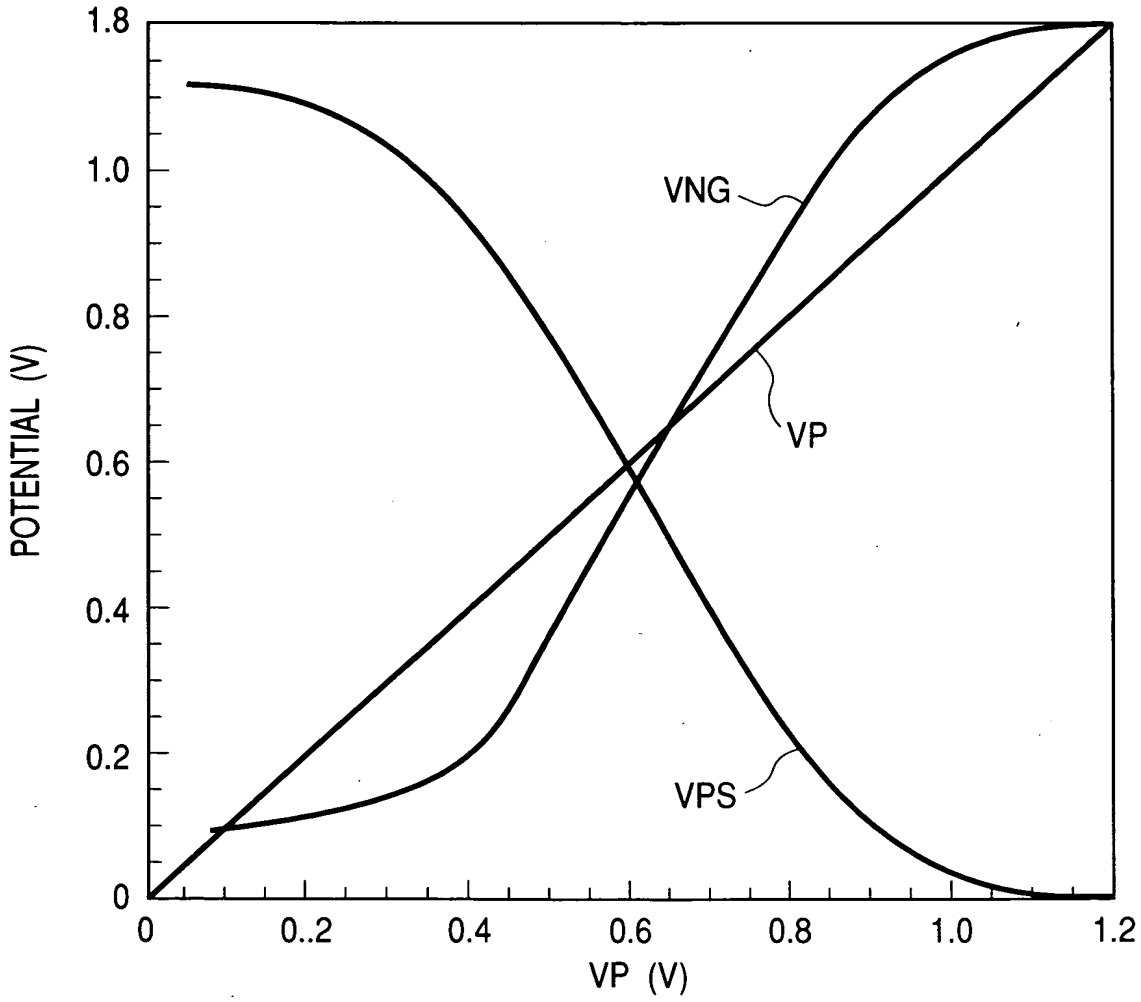


FIG. 9(a)

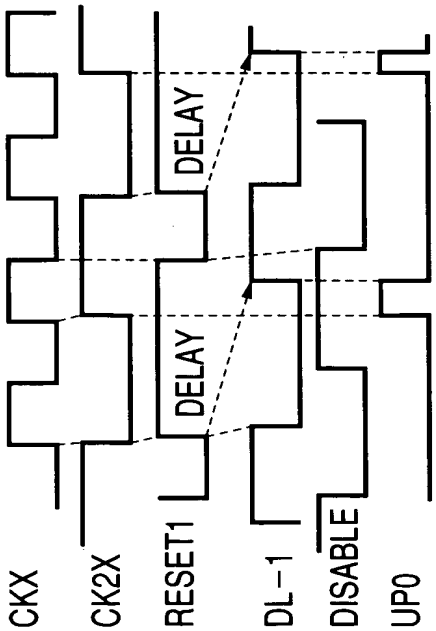


FIG. 9(b)

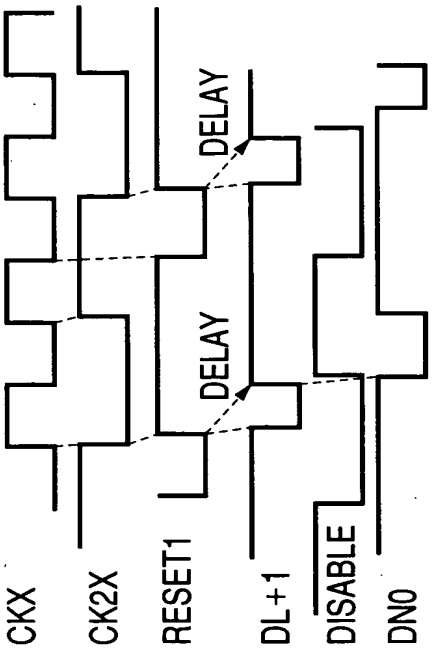


FIG. 9(c)

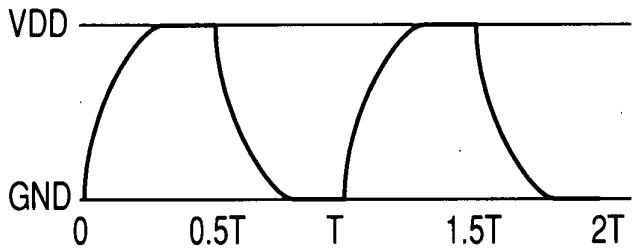
FIG. 9(d)

FIG. 10(a)

WITH ONLY THE VARIABLE DELAY CIRCUIT
AMOUNT OF DELAY = OPERATION PERIOD

OPERATION TARGET PERIOD = 2 ns TO 10 ns

OPERATION RANGE OF ONE STAGE OF
VARIABLE DELAY CIRCUIT = 0.2 ns TO 10 ns
MAXIMUM DELAY/MINIMUM DELAY RATIO = 5

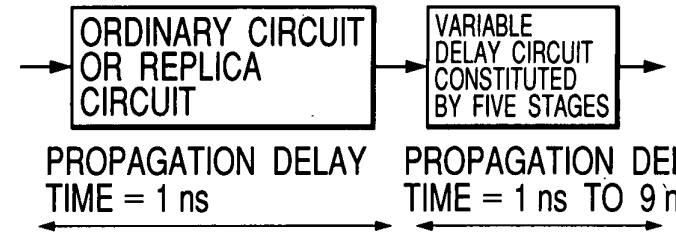


EXAMPLE OF WAVEFORM WITHIN THE VARIABLE DELAY CIRCUIT UNDER THE MAXIMUM DELAY CONDITION

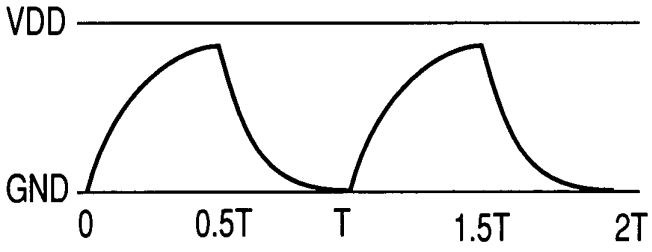
FIG. 10(b)

WITH VARIABLE DELAY CIRCUIT + INTERNAL CIRCUIT
AMOUNT OF DELAY = OPERATION PERIOD

OPERATION TARGET PERIOD = 2 ns TO 10 ns

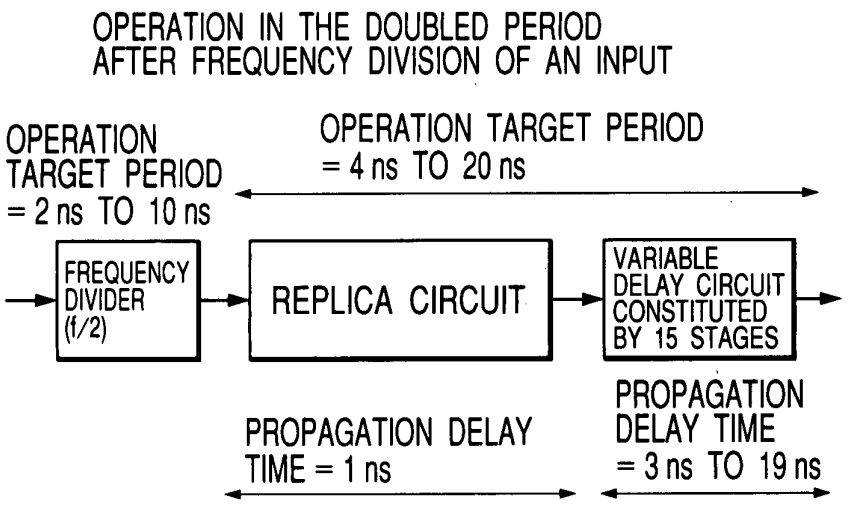


OPERATION RANGE OF ONE STAGE OF
VARIABLE DELAY CIRCUIT = 0.2 ns TO 1.8 ns
MAXIMUM DELAY/MINIMUM DELAY RATIO = 9



EXAMPLE OF WAVEFORM WITHIN THE VARIABLE DELAY CIRCUIT UNDER THE MAXIMUM DELAY CONDITION

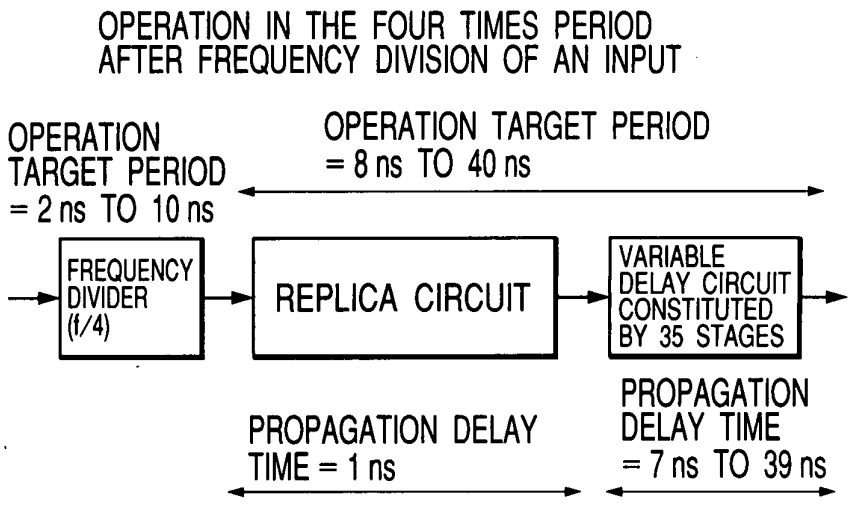
FIG. 11(a)



OPERATION RANGE OF ONE STAGE OF VARIABLE DELAY CIRCUIT = 0.2 ns TO 1.27 ns

MAXIMUM DELAY/MINIMUM DELAY RATIO = 6.33

FIG. 11(b)



OPERATION RANGE OF ONE STAGE OF VARIABLE DELAY CIRCUIT = 0.2 ns TO 1.11 ns

MAXIMUM DELAY/MINIMUM DELAY RATIO = 5.55

FIG. 12

EXAMPLE OF STRUCTURE OF VARIABLE DELAY CIRCUIT 2
(IN THE CASE OF 1/4 FREQUENCY DIVISION)

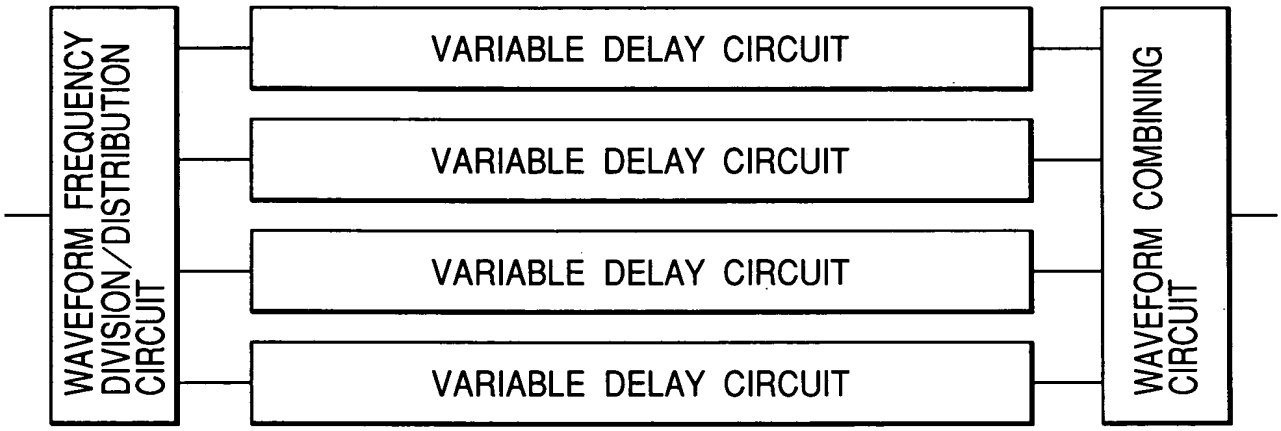


FIG. 13

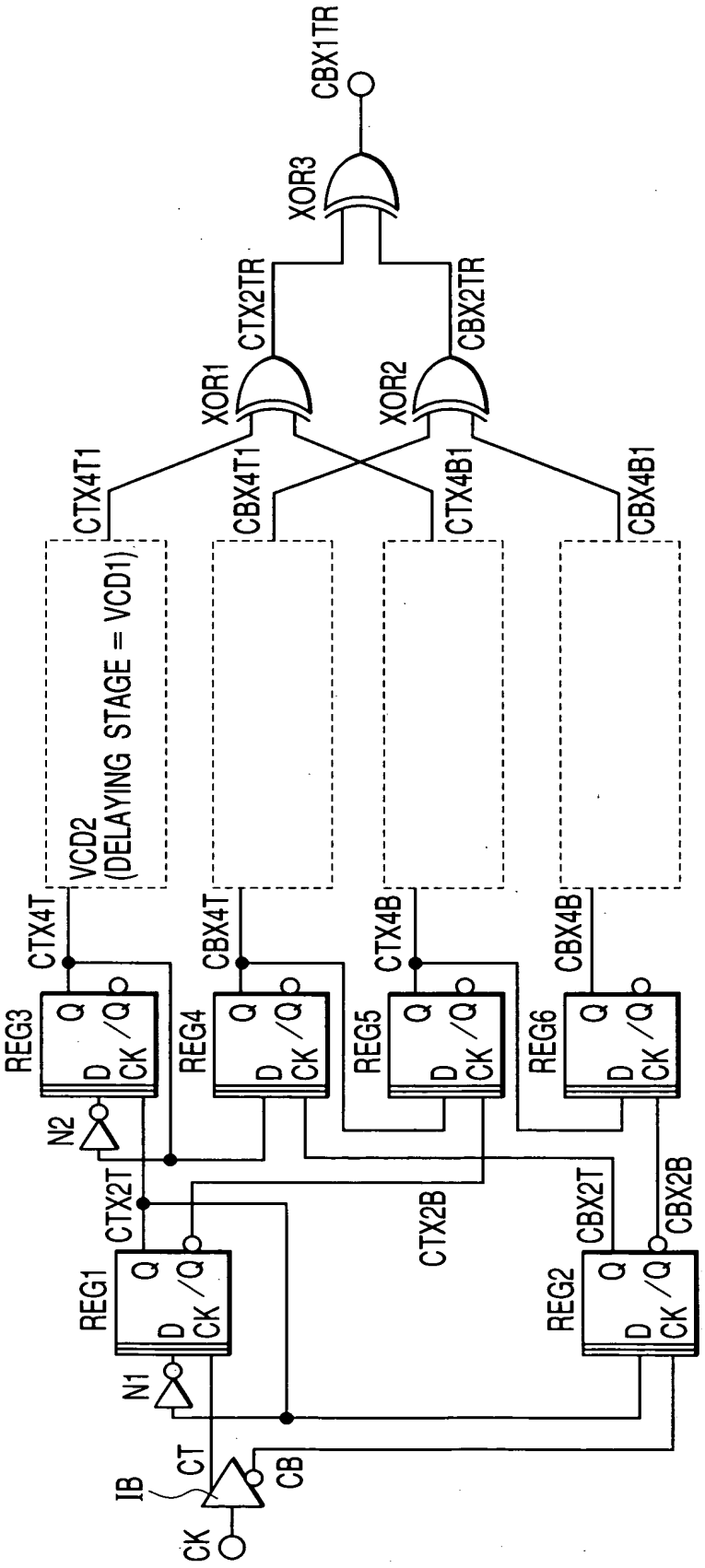

CBX1TR
XOR3
CTX2TR
CBX2TR
XOR1
XOR2
CTX4T1
CBX4T1
CTX4B1
CBX4B1
VCD2
(DELAYING STAGE = VCD1)
CTX4T
CBX4T
CTX4B
CBX4B
REG3
REG4
REG5
REG6
Q
/Q
D
CK
N2
CTX2T
CTX2B
CBX2T
CBX2B
REG1
REG2
N1
IB
CT
CB
CK

FIG. 14

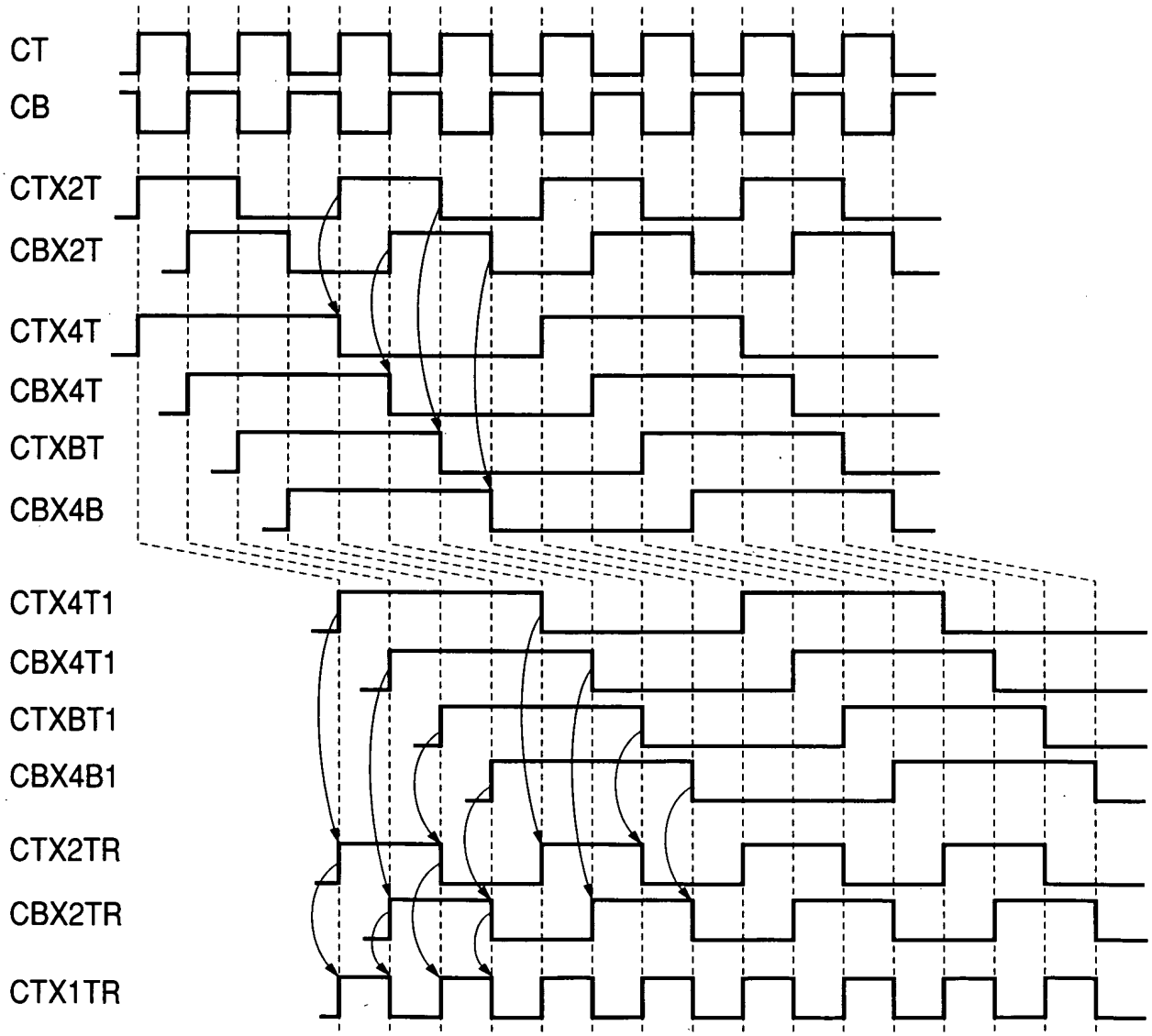

CT
CB
CTX2T
CBX2T
CTX4T
CBX4T
CTXBT
CBX4B
CTX4T1
CBX4T1
CTXBT1
CBX4B1
CTX2TR
CBX2TR
CTX1TR

FIG. 15

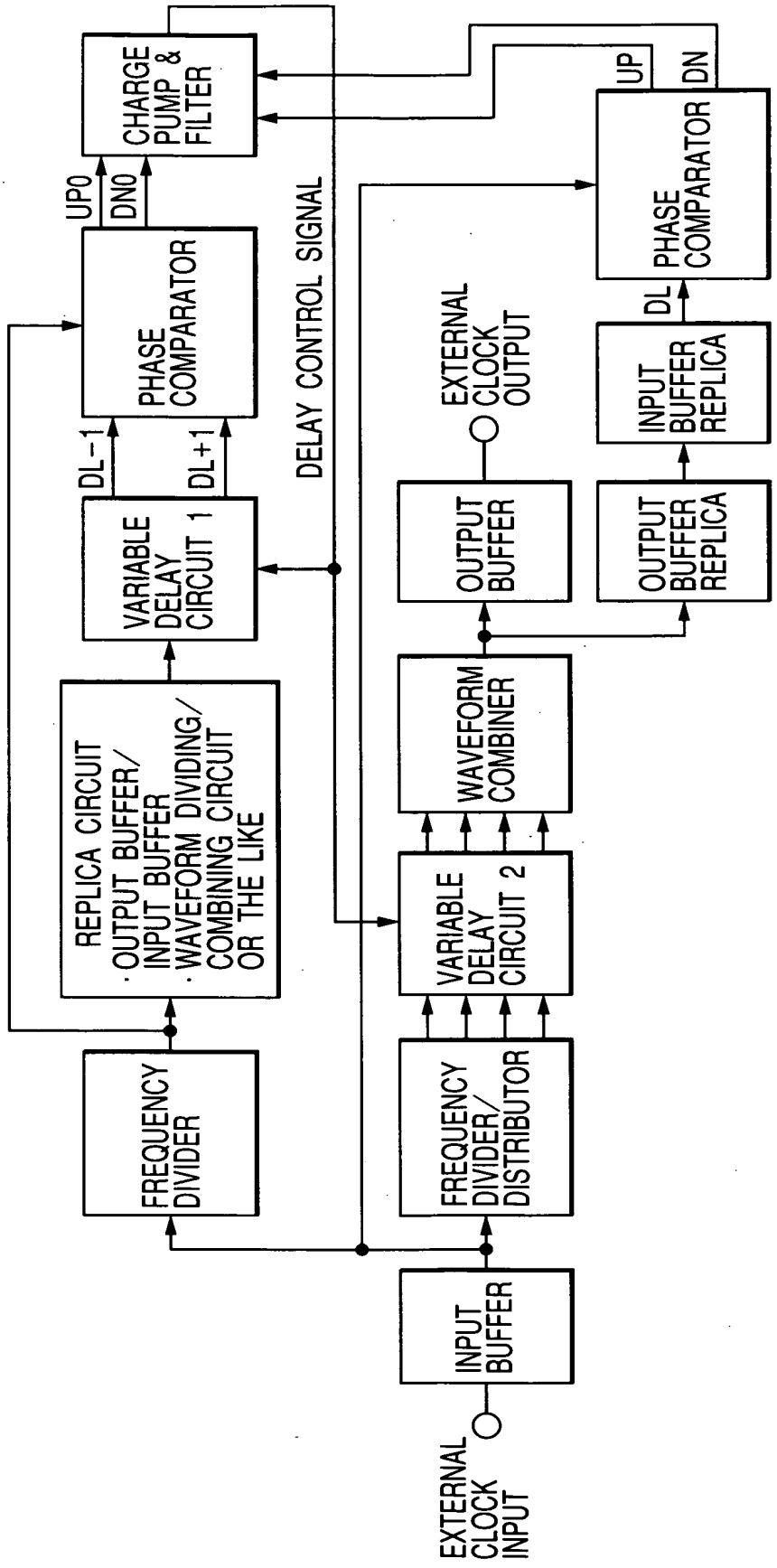

EXTERNAL CLOCK INPUT
INPUT BUFFER
FREQUENCY DIVIDER/ DISTRIBUTOR
FREQUENCY DIVIDER
VARIABLE DELAY CIRCUIT 2
VARIABLE DELAY CIRCUIT 1
REPLICA CIRCUIT · OUTPUT BUFFER/ INPUT BUFFER · WAVEFORM DIVIDING/ COMBINING CIRCUIT OR THE LIKE
WAVEFORM COMBINER
OUTPUT BUFFER
OUTPUT BUFFER REPLICA
EXTERNAL CLOCK OUTPUT
INPUT BUFFER REPLICA
DL
PHASE COMPARATOR
UP
DN
CHARGE PUMP & FILTER
UP0
DN0
PHASE COMPARATOR
DL−1
DL+1
DELAY CONTROL SIGNAL

FIG. 16

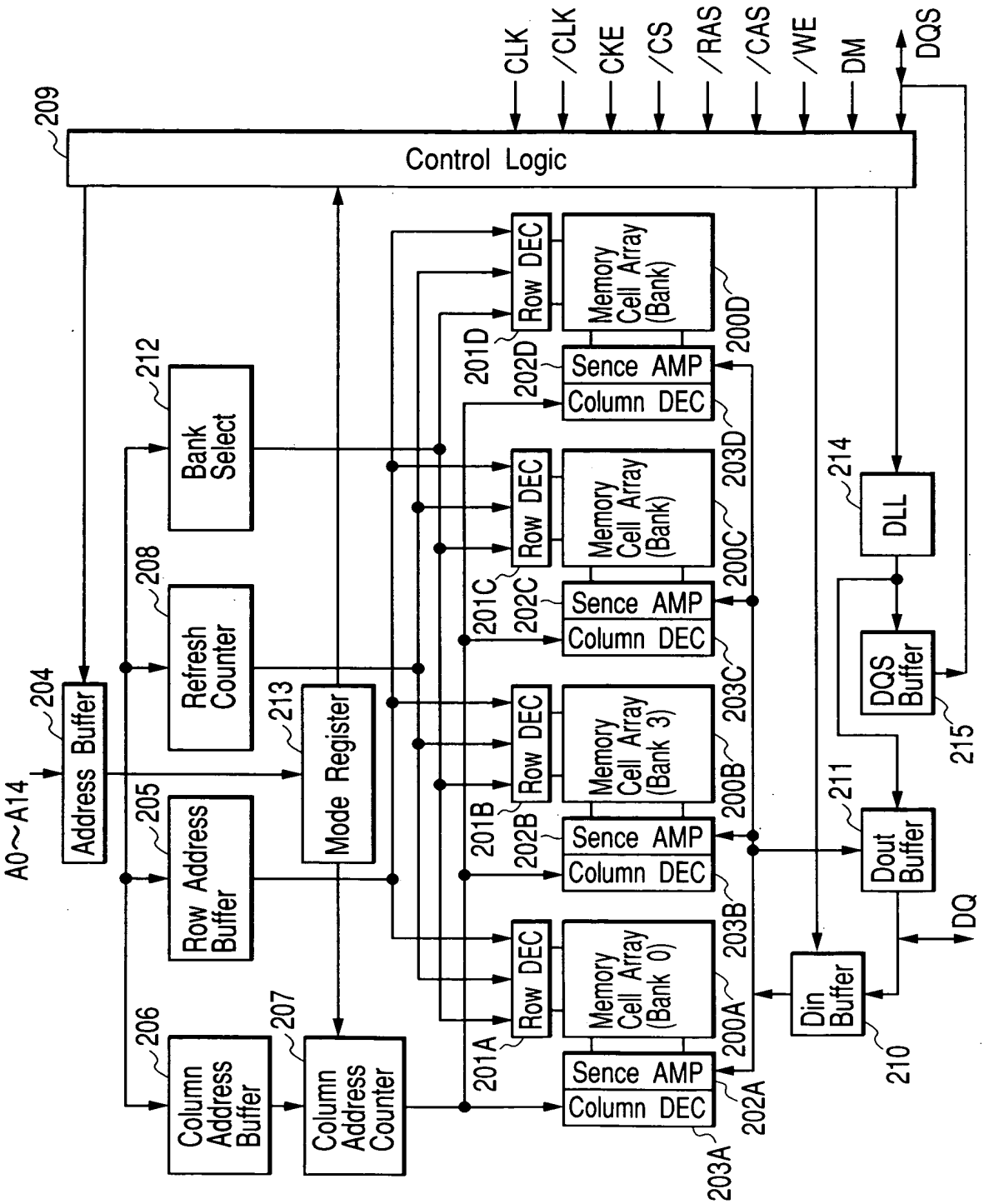
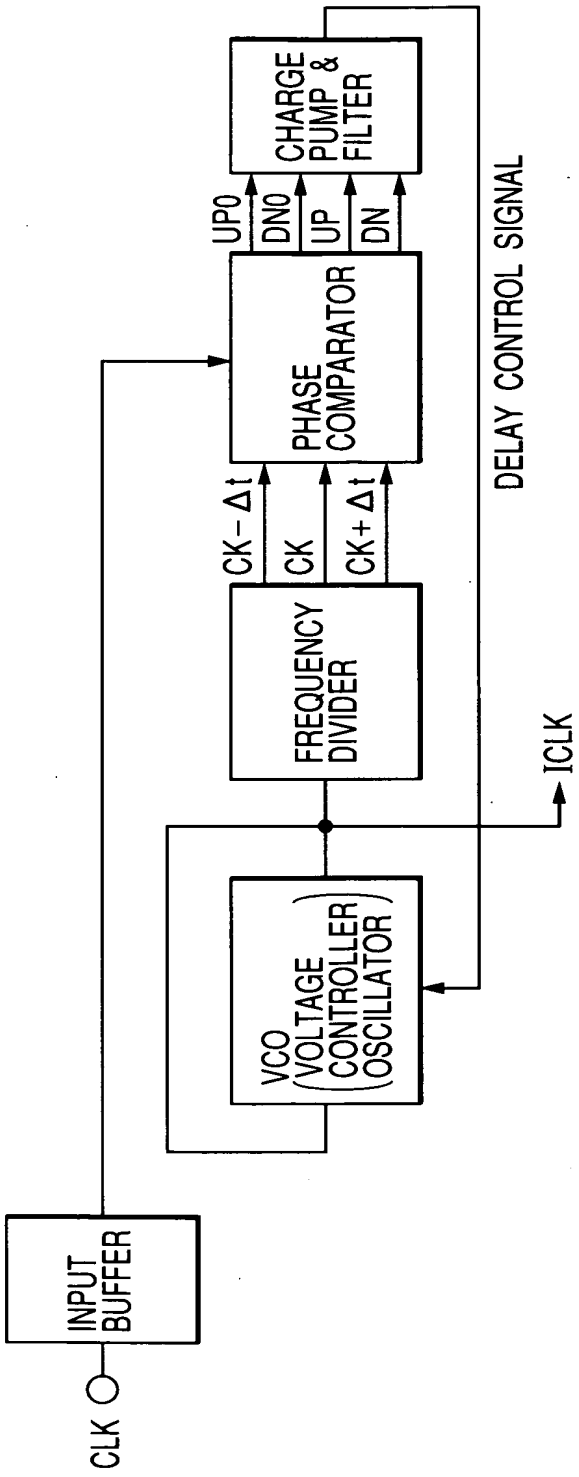

CLK
/CLK
CKE
/CS
/RAS
/CAS
/WE
DM
DQS
209
Control Logic
212
Bank Select
208
Refresh Counter
213
Mode Register
204
Address Buffer
A0~A14
205
Row Address Buffer
206
Column Address Buffer
207
Column Address Counter
Row DEC
Memory Cell Array (Bank)
Sence AMP
Column DEC
201D
202D
200D
203D
201C
202C
200C
203C
Memory Cell Array (Bank 3)
201B
202B
200B
203B
Memory Cell Array (Bank 0)
201A
202A
200A
203A
214
DLL
DQS Buffer
215
Dout Buffer
211
Din Buffer
210
DQ

FIG. 17


CLK
INPUT BUFFER
VCO (VOLTAGE CONTROLLER OSCILLATOR)
FREQUENCY DIVIDER
PHASE COMPARATOR
CHARGE PUMP & FILTER
CK− Δt
CK
CK+ Δt
UP0
DN0
UP
DN
DELAY CONTROL SIGNAL
ICLK